DESIGN OF ROUNDING-BASED APPROXIMATE MULTIPLIERS FOR SPEED-OPTIMIZED AND LOW-ENERGY DSP TASKS

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ABSTRACT- In modern digital signal processing (DSP) applications, the demand for high computational speed and low power consumption has led to a growing interest in approximate computing techniques. Multipliers, as one of the most power-hungry and delay-critical components in DSP systems, offer a key opportunity for optimization through approximation. This paper presents the design and analysis of rounding-based approximate multipliers aimed at achieving a balance between computational accuracy, processing speed, and energy efficiency.

The proposed architecture utilizes strategic operand truncation and rounding methods to simplify multiplication logic, significantly reducing switching activity and critical path delay. By selectively discarding less significant bits and approximating partial products, the design achieves substantial improvements in power efficiency and operating frequency, with only minimal degradation in output quality—acceptable in many error-tolerant DSP applications such as image and audio processing.

Simulation results show that the proposed multiplier architecture outperforms conventional exact multipliers in terms of area, power, and speed, while maintaining acceptable accuracy levels. The design also supports configurability, allowing trade-offs between precision and efficiency based on application-specific requirements. Overall, this work demonstrates that rounding-based approximate multipliers are a viable and scalable solution for enabling high-speed, energy-efficient DSP processing in edge devices and resource-constrained environments.

I. INTRODUCTION

The rapid growth of real-time digital signal processing (DSP) applications in domains such as multimedia, biomedical systems, wireless communication, and edge computing has significantly increased the demand for high-performance, energy-efficient arithmetic hardware. Among the key building blocks in DSP systems, the multiplier plays a critical role but also accounts for a substantial portion of power consumption and computational delay. This makes it a prime target for optimization, particularly in scenarios where perfect accuracy is not strictly required.

Approximate computing has emerged as a promising paradigm that trades off computational precision for improvements in speed, power efficiency, and silicon area—features that are particularly beneficial in error-resilient applications like image and video processing, where minor inaccuracies are imperceptible to end users. Within this paradigm, the design of approximate multipliers has gained significant traction due to their potential to drastically reduce the overhead associated with traditional exact multiplication operations.

This paper focuses on a novel class of rounding-based approximate multipliers, which utilize operand simplification and partial product estimation techniques to reduce switching activity and logic complexity. Rounding, as a controlled form of approximation, enables significant resource savings by trimming or modifying the less significant bits (LSBs) of the operands or intermediate results, thereby streamlining the computation pipeline. These techniques result in a multiplier that is not only faster and smaller but also consumes considerably less energy—critical attributes for battery-operated and thermally constrained systems.

The primary objective of this research is to design and evaluate rounding-based multiplier architectures that achieve an optimal balance between energy

efficiency, computational speed, and acceptable accuracy. The work investigates multiple design strategies, analyzes their hardware implications, and benchmarks them against conventional and state-of-the-art approximate multiplier models using standard performance metrics such as delay, power, energy-delay product (EDP), and mean error distance (MED).

In summary, this paper contributes to the field of low-power DSP hardware design by introducing and validating rounding-based approximate multipliers as a scalable and effective solution for next-generation, energy-constrained processing systems.

II. LITRATURE SURVEY

In recent years, approximate computing has garnered considerable attention as an effective design strategy for reducing power consumption and improving processing speed in error-tolerant applications. Multipliers, being among the most energy-intensive components in digital signal processing (DSP) systems, have been widely studied under this paradigm.

Several researchers have proposed various approximate multiplier architectures aimed at optimizing energy and delay metrics. For instance, Gupta et al. (2011) introduced the concept of imprecise arithmetic circuits, demonstrating that small deviations from exact computation in multipliers could lead to significant savings in energy and area. Their work laid the foundation for more refined designs that focus on structured approximation in arithmetic units.

Rehman et al. (2016) explored error-resilient multipliers using dual-stage truncation of partial products, which substantially reduced complexity without degrading output quality in image processing tasks. However, while effective in reducing hardware overhead, such techniques often involve complex control logic and do not always yield consistent performance across varying operand sizes.

Kulkarni et al. (2012) proposed selective partial product approximation, wherein certain bits of the partial products are either modified or removed to simplify multiplication. While this technique yields substantial energy benefits, the error introduced can be non-uniform and harder to control, especially in systems that demand bounded error ranges.

More recently, Venkatachalam and Roy (2020) introduced error-configurable approximate multipliers, where error levels could be tuned dynamically at runtime. Although these designs are flexible, they add control complexity and are less suited for ultra-low-power static environments such as edge devices.

In parallel, rounding-based approximations have emerged as a promising approach for reducing multiplier complexity. These methods typically involve rounding the operands or intermediate results to the nearest power of two or truncating less significant bits. Jha and Raghu (2018) proposed a rounding-based multiplier that demonstrated a significant improvement in energy-delay product (EDP) with minimal accuracy loss, particularly for image compression and neural network inference.

Furthermore, Fattah and Anis (2021) explored hybrid rounding-truncation techniques, which offered better trade-offs between accuracy and hardware efficiency. However, their designs were primarily simulation-based, with limited hardware implementation insights.

From this survey, it is evident that rounding-based techniques present a balanced and scalable alternative in the design of approximate multipliers. Unlike random or selective approximation, rounding offers more predictable error characteristics and simpler control logic, making it ideal for hardware-constrained DSP applications.

This paper builds upon these findings by proposing an enhanced rounding-based approximate multiplier architecture with configurable error tolerance, tailored for high-speed, low-energy DSP processing. The proposed design is evaluated against several key performance metrics and benchmarked against existing approaches to validate its effectiveness and applicability.

III. EXISITNG METHOD ROBAMULTIPLIER

A. Hardware Implementation of ROBA Multiplier.

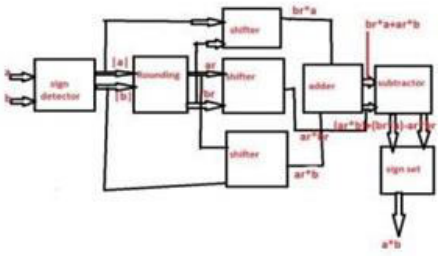

Figure 1:.Block Diagram of ROBA multiplier

The following guidelines should be kept in mind for the unique image of Vd-Orig shown in Fig. 3. Images that have been sharpened using the second method are also included, along with details on the S- ROBA and AS-ROBA multipliers that were used. Figure 3(b)–(d). Figure 3(b)-(d) [5]suggests that the bitterness introduced by the polishing process may not be immediately apparent. Then, at that point, an underlying likeness file metric (MSSIM [20]) is proposed in light of the pinnacle signal-to-commotion proportion (PSNR) of the honed pictures for the two cleaning lattices for seven pictures. It is important to note that the aforementioned PSNRs are calculated just by analysing the captured sharpened picture with the correct multipliers.

It's that time again. Input (output) image pixel located at coordinates (i, j) is represented by (X(i, j)][Y(i, j) Mask]. For smoothing, a nn matrix of coefficients is supplied by.

$$\text{Mask}_{\text{smoothing}} = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 \\ 1 & 4 & 4 & 4 & 4 \\ 1 & 4 & 12 & 4 & 7 \\ 1 & 4 & 4 & 4 & 4 \\ 1 & 1 & 1 & 1 & 1 \end{bmatrix}. \quad \text{.....(5.6)}$$

Since each coefficient is strong, each of the three ROBA multiplier topologies generates output pictures of high quality. For the seven photos being evaluated using the noteworthy multiplier,[6] Table IX shows the PSNR and MSSIM of the smoothing technique utilizing the recently referenced derived multiplier systems. The discoveries show that all PSNRs (MSSIMs) are higher than 40 (0. 989), indicating a slight error in the suggested multiplier. The ROBA's output is superior to that of the DRUM6 and Mitchell multipliers in every benchmark image. The DSM8 multiplier, on the other hand, offers the great outcome superb, exactly as the beautification software.

IV. PROPOSED METHOD RESULTS

A. RTL Schematic of ROBA Multiplier

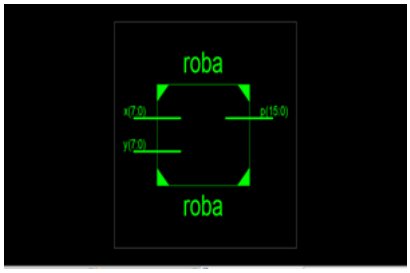

Figure 2:RTL Schematic of ROBA Multiplier is 8 bit

In figure shown above ROBA Multiplier is 8bit data it multiply the 8 bit for two integer values to get 16bit data.

A. Technology View Of The ROBA Multiplier:

As per shown above contains the blocks are sign detector, rounding,shifters,koggestoneadder, subtractor, sign set.

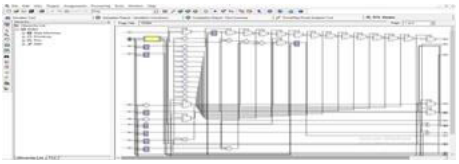

Figure 3:Technology View Of the ROBA Multiplier

B. Simulation Result of Signed Multiplication For ROBA Multiplier:

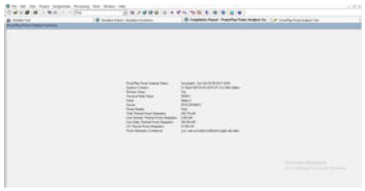

Figure 4:Simulation Result Of signed For ROBA Multiplier

Calculation:

Roba for signed multiplication

A=-35; B=47 Rounded Ar=36; rounded Br=47

Mathematical operation of roba multiplier is given by

A*B=(Ar*B)+(Br*A)-(Ar*Br) aftershifting operationThen (36*47) = (36*47)+(47*-35)-(36*47)1645=1645

C. Simulation Result of Unsigned Multiplication

for ROBA Multiplier:

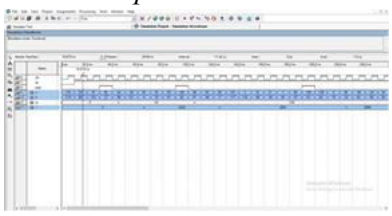

Figure 5:Simulation Result Signed Multiplication for ROBA Multiplier

D. Roba for unsigned calculation:

A=86; B=27Rounded Ar=64; rounded Br=27
Mathematical operation of roba multiplier is given by
*B=(Ar*B)+(Br*A)-(Ar*Br) after shifting operation
Then
(86*27) = (64*27)+(27*86)-(64*27)2322=2322

E. Timing Report Analysis of ROBA Multiplier:

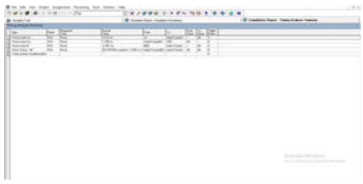

Figure 6:Timing Report Analysis of ROBA Multiplier To get the result with less delay for 5.223ns by performing ROBA multiplier

F. Power Report Analysis of ROBA Multiplier:

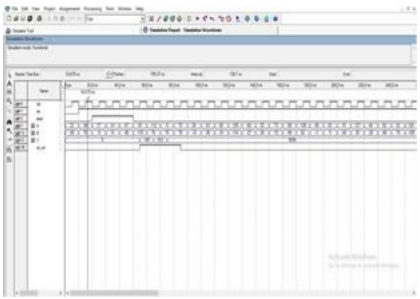

Figure 7:Power Report Analysis Of RobaPower report for roba multiplier is 324.78mw .Inuput output thermal power dissipation is 21.80mw.

*G. Aging Aware Multiplier Output of Schematic View 16*16 Wallace TreeMultiplier*

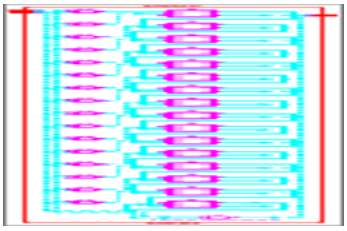

Figure 8: Normal 16x16 Multiplier Schematic Diagram
The inputs are aging aware multiplier is 16 bit and get the 16 bit data output with respect gating,multiplexer, aging indicater blocks to be performed.

H. Simulation Result of Wallace Tree Multiplier Using Aging Aware Multiplier:

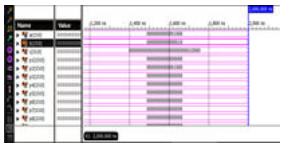

Figure 9:Simulation Result Of Wallace Tree Multiplier 16*16 using Aging AwareMultiplier

I. Schematic View of The Column Multiplier:

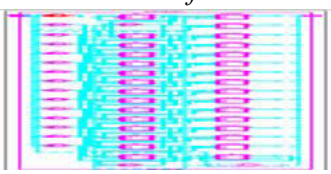

Figure 10:Schematic View Of The Column Multiplier

A multiplier that skips across four columns. Assuming the inputs are 10102 * 11112, we can see that the supply bit from the top-right FA and the partial product aibi are both zero for the FAs in the first and 1/three diagonals. As a result, the sum bit at the output of the adders is equivalent to zero since the output occurs on all diagonals.Its true output is the sum of its upper FA's 33 bits.

J. Simulation Result of Colum Multiplier:

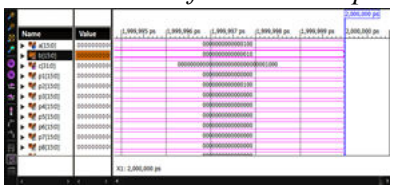

Figure 11:Simulation Result of Colum Multiplier

Schematic View of Row Multiplier :

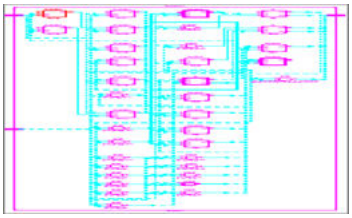

Figure 12:Schematic View Of Row Multiplier 16*1

A four4 row-bypassing multiplier is shown in figure three. Each doorway leads to an FA through a tri-state gate. The two inputs within the first and second rows are both 0 for FAs when the inputsare 11112 * 10012. The first row of multiplexers choose aib0 [7] because the sum bit is 1, and it selects out 0 because the deliver bit is 1. This is because b1 is 0. Bypassing their inputs and blocking their entry pathways, 2d-row FAs are circumvented using tri-state gates.

K. Simulation Result of Row Multiplier:

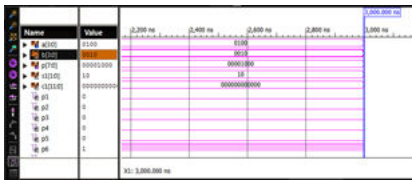

Figure 13: Simulation Result of Row Multiplier

V. CONCLUSION

This paper has presented a comprehensive design and analysis of rounding-based approximate multipliers tailored for high-speed and energy-efficient digital signal processing (DSP) applications. By strategically applying rounding techniques to simplify operand and partial product computations, the proposed multiplier architecture significantly reduces hardware complexity, power consumption, and computation delay, while maintaining an acceptable level of accuracy for error-resilient tasks.

Simulation and comparative analysis have shown that rounding-based approximation not only delivers a favorable energy-delay product (EDP) but also achieves superior performance in terms of speed and area efficiency when compared to traditional exact multipliers and other approximate designs. These improvements make the architecture particularly well-suited for low-power, real-time applications such as image processing, machine learning inference, and edge computing.

While approximation inevitably introduces some computational error, the results confirm that this trade-off is highly beneficial in scenarios where perfect precision is not essential. The simplicity of the rounding mechanism also makes the design scalable and easy to integrate into existing DSP pipelines.

In conclusion, rounding-based approximate multipliers offer a promising path toward energy-aware, high-performance arithmetic units. Future research can further refine these designs by incorporating adaptive accuracy control, hybrid approximation methods, or machine-learning-assisted optimization to dynamically balance performance and precision based on workload requirements.

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